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HB

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
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08/997,035	12/23/97	FUDANUKI	N 040301/0487
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MM42/0727

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EXAMINER

LE.D

ART UNIT

PAPER NUMBER

2819

5

DATE MAILED: 07/27/99

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application No.
08/997,035

Applicant(s)
Fudanuki

Examiner
Don Le

Group Art Unit
2819



☐ Responsive to communication(s) filed on _____.

☐ This action is **FINAL**.

☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire 3 month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claims

☒ Claim(s) 1-23 is/are pending in the application.

Of the above, claim(s) _____ is/are withdrawn from consideration.

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) 1-23 is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☒ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☒ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☒ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been
☒ received.

☐ received in Application No. (Series Code/Serial Number) _____.

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____.

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☒ Notice of References Cited, PTO-892 ✓

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). _____

☐ Interview Summary, PTO-413

☒ Notice of Draftsperson's Patent Drawing Review, PTO-948 ✓

☐ Notice of Informal Patent Application, PTO-152

--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---

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Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 3, 4, 14 and 15 are rejected under 35 U.S.C. 102(b) as being anticipated by Gould et al. (US 5,051,917).

3. With respect to claim 1, figures 1 and 6 of Gould show an integrated circuit comprising:
a plurality of cell rows (figure 1), in each row a plurality of standard cells (22 and 58) are arranged; and

gate array basic cells (54 and 56) formed in an empty space of a predetermined cell row of the plurality of cell rows.

4. With respect to claim 3, figure 1 of Gould further shows the gate array basic cells formed in wiring channel regions disposed between the plurality of cell rows. (Wiring between cells can be accomplished to the purpose of forming logical function. As a result, the basic cells are located in the wiring channel).

5. With respect to claim 4, figure 1 of Gould shows the cell rows are arranged adjacently.

6. With respect to claims 14 and 15, figure 6 of Gould shows the standard cells and the basic cells are arranged pursuant to a same grid system.

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Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. Claims 2, 5-9, 11-13 and 16-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gould et al.

9. With respect to claims 2 and 5, figure 6 of Gould shows the standard cells and the basic cells are arranged in a rectangular pattern. However, the apparatus of Gould does not specifically show the standard cells having a height substantially identical to that of the basic cells. It is well known in the art that basic cells and standard cells can be manufactured to have a certain height as a matter of design choice. It would have been obvious to one of ordinary skill of art at the time the invention was made to have the manufactured the height of the standard cells and basic cells of Gould to be substantially equal as a matter of design choice.

10. With respect to claims 6 and 7, figure 1 of Gould shows the standard cells and the basic cells are arranged adjacently along a direction orthogonal to the cell rows.

11. With respect to claims 8, 9 and 11, the apparatus of Gould does not specifically show the standard cells and the basic cells having common signal lines. It is well known in the art that connection between cells can be made in order to formed the cells into a logical circuit. It would have been obvious to one of ordinary skill of art at the time the invention was made to have the

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basic cell and the standard cells connected to common signal lines as a matter of design choice for the purpose of forming a logical circuit using the basic cells and the standard cells.

12. With respect to claims 12 and 13, figure 6 of Gould shows the standard cells are integral multiple of a width of the basic cells.

13. With respect to claims 16-19, the apparatus of Gould does not specifically show the basic cells are used to construct an intermediate clock buffer or additional circuits as claimed by applicant. It is well known in the art that basic cells can be designed to be a buffer or additional circuits and buffers can be used to distribute a clock signal to a plurality of circuits in the integrated circuit or additional circuit can be used for the purpose increase driving capability of the integrated circuit. It would have been obvious to one of ordinary skill of art at the time the invention was made to have used the basic cells of Gould to design into a buffer for the purpose of distributing a clock signal in the integrated circuit or used the basic cells to design into additional circuits for the purpose of increase driving of the integrated circuit as a matter of design choice.

14. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gould et al. as applied to claim 2 above, and further in view of Kitamura et al. (US 4,811,073).

15. With respect to claim 10, the apparatus of Gould does not specifically show the standard cells and the basic cells having common power supply lines. Figure 3 of Kitamura shows an integrated circuit having gate array comprising of basic cells (10) having common power lines (PDD and PSS) for the purpose of providing minimal power lines connecting to each of the basic

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cells. It would have been obvious to one of ordinary skill of art at the time the invention was made to have the standard cells and the basic cells of Gould connected to common power lines as taught by kitamura for the purpose of having minimum power lines in an integrated circuit.

16. Claims 20-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gould et al. In view of applicant prior art figure 2.

17. With respect to claim 20, figures 1 and 6 of Gould show a logic circuit area comprising:
a plurality of cell rows (figure 1), in each row a plurality of standard cells (22 and 58) are arranged; and

gate array basic cells (54 and 56) formed in an empty space of a predetermined cell row of the plurality of cell rows.

The apparatus of Gould does not specifically shows the logic circuit is used as part of an integrated circuit having a megacell and a megafunction. Applicant prior art figure 2 shows an integrated circuit having megacell (213), megafunction (211) and a logic circuit area (221 and 222) in a single integrated circuit for the purpose of providing an integrated circuit on one chip. It would have been obvious to one of ordinary skill of art at the time the invention was made to have used the logic circuit area of Gould in place of the logic area of applicant prior art figure 2 as a matter of design choice.

18. With respect to claim 21, figure 6 of Gould shows the standard cells and the basic cells are arranged in a rectangular pattern. However, the apparatus of Gould does not specifically show the standard cells having a height substantially identical to that of the basic cells. It is well known

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in the art that basic cells and standard cells can be manufactured to have a certain height as a matter of design choice. It would have been obvious to one of ordinary skill of art at the time the invention was made to have the manufactured the height of the standard cells and basic cells of Gould to be substantially equal as a matter of design choice.

19. With respect to claim 22, figure 1 of Gould further shows the gate array basic cells formed in wiring channel regions disposed between the plurality of cell rows. (Wiring between cells can be done. As a result, the basic cells are located in the wiring channel).

20. With respect to claim 23, figure 6 of Gould shows the standard cells and the basic cells are arranged pursuant to a same grid system.

Prior Art

21. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

A. Nonaka (US 4,949,275) discloses an integrated circuit having standard cells and basic cells.

B. Ando et al. (US 4,969,029) disclose an integrated circuit having basic cells.

C. Okutsu et al. (US 4,967,100) disclose an integrated circuit having standard cells and basic cells.

D. Suguyama et al. (US 4,207,556) disclose an integrated circuit having standard cells and basic cells.

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E. Matsumura et al. (US 4,809,029) disclose an integrated circuit having basic cells and standard cells.

F. Hickman et al. (US 5,155,390) disclose an integrated circuit various types of cells.

G. Asami (US 4,750,027) discloses an integrated circuit having standard cells and basic cells.

Conclusion

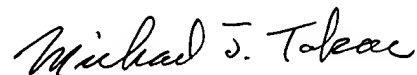
8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Don Le, whose telephone number is (703) 308-4890. Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703)308-0956.



Don Le

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July 22, 1999



Michael J. Tolcar
Supervisory Patent Examiner
Technology Center 2800